A 64 Gb DDR4 STT MRAM using Timing Controlled Discharging reading scheme for 1Selector 1MTJ cross point cell of 0.001681 um^2

A. Katayama[1*], K. Hatsuda[1], K. Hoya[1], R. Takizawa[1], F. Matsuoka[1], T. Yasuda[1], T. Miyakawa[1], K. Senju[1], K. Okawa[1], Y. Furukawa[1], Y. Shimada[1], K. Kotake[1], S. Hirokawa[1], M.C. Shin[2], D.K. Kim[2], T.H. Kim[2], K. Kim[2], H. Aikawa[3], J. Song[2], T. Nagase[3], S.M. Seo[2], S.G. Kim[2], J. Yi[2], and S.Y. Cha[2]

[1]KIOXIA Corp., Yokohama, Japan
[2]SK hynix Inc., Icheon, Republic of Korea
[3]KOXIA Korea Corp., Seoul, Republic of Korea

Recent rapid demand for new applications such as A.I., database processing, big data processing, or real time applications enhances the development of Storage Class Memory (SCM) targeting high density, low latency and high reliability. Many devices for SCM such as Phase Change Memory (PCM), Resistive RAM (RRAM), Selector Only Memory (SOM) have been developed intensively. PCM has been already commercialized once and SOM as improved devices of PCM has been developed by many organizations recently.[1]. Meanwhile, STT-MRAM device also has widely commercialized for non-volatile memory such as eMRAM macro [2] or standalone MRAM chip [3], because of its low power consumption and fast write speed operation. In this paper, we demonstrate a new reading scheme "Timing Controlled Discharging" combined with "Local capacitance mode" to realize high density cross point STT-MRAM targeting SCM as well as high density 64Gb STT-MRAM with 20.5nm HP 1S1M cell (0.001681um2)[4-6] . For the first time, we demonstrate reliable read/write operation in 1S1M cell arrays.

Fig.1 shows cross point architecture of realizing the high density MRAM. This cross sectional view shows the cross point array which consists of MTJ and selector elements and also Peripheral Under Cell (PUC) structure of this work. This cross point array realizes the world's smallest 4F2 cell by connecting MTJ and selector in series and peripheral circuits such as switches, read/write circuits and other logics are placed in PUC. Cell array size can be expanded at 4k Word lines (WL) and 2k Bit lines (BL) by optimizing PUC layout topology.

Fig.2 shows a novel design technique for reading celled "Timing Controlled Discharging" reading (TCDR) scheme in this work. In most of the reported MRAMs, a cell signal is detected by applying a constant current (CC) or a constant voltage (CV) to a cell. However, conventional reading schemes have several severe issues such as inducing read disturbance and unstable reading due to using selector in cross point architecture.

Our new proposed reading scheme enables to suppress read disturbance and realize a stable reading by discharging pre-charged charges at BL to WL through cell without applying the CC and CV as shown Fig. 2. This scheme can also eliminate the constraint of selector's properties such as Ihold and cell size scaling. Furthermore, by combining the "Local capacitance mode" that makes parasitic capacitance reduced, reliable read/write operation in 1S1M cell arrays is achieved for the first time.

References

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* Corresponding author: email: akira4.katayama@kioxia.com

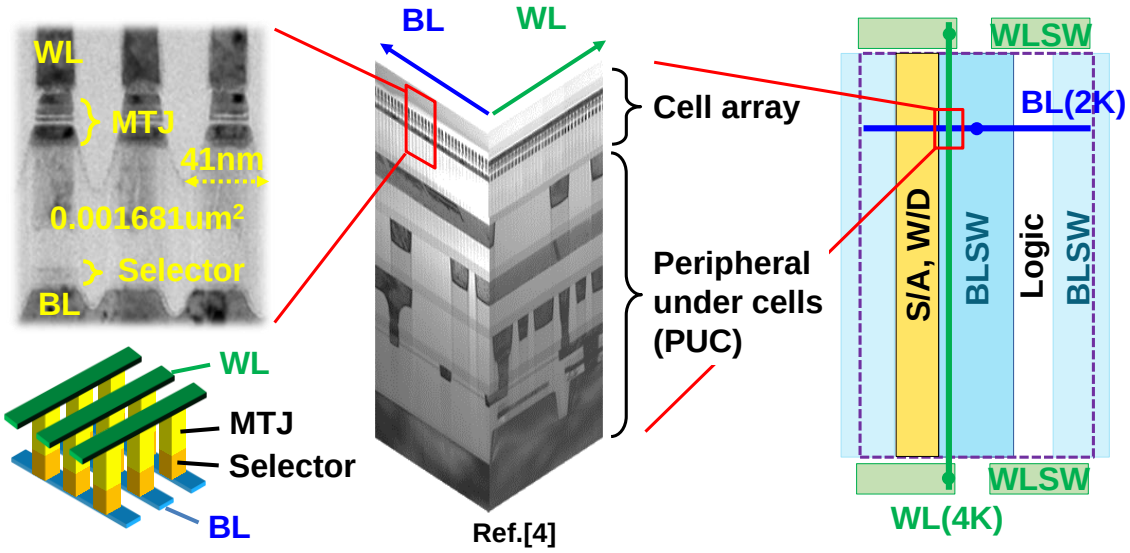
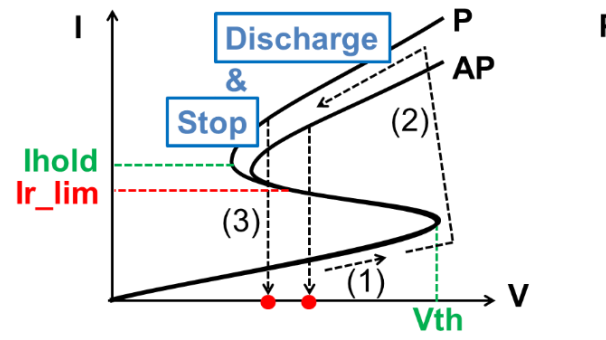


Fig. 1: Cross-sectional TEM image and core architecture for cell array and peripheral under cells.[6] ©2025 IEEE



	Signal Stability	Read Disturb	Condition at sense
CC	×	△～×	Oscillation
CV	○	×	Large current flow
TCDR	○	○	No current and stable

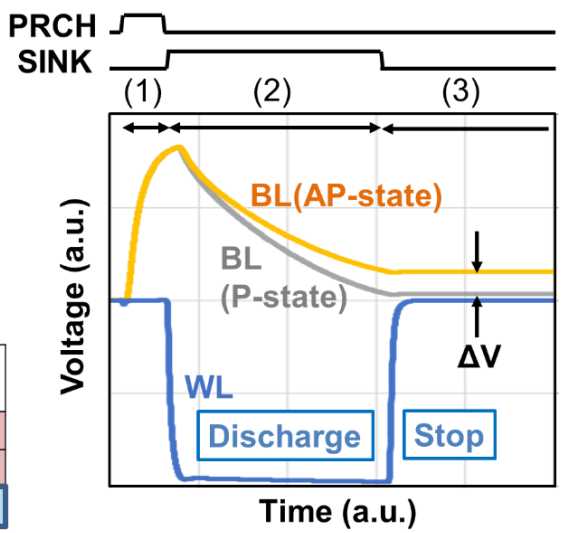


Fig. 2: The operating for the proposed read scheme, and the simulation waveforms of the proposed reading scheme. [6] ©2025 IEEE